

REMARKS

As an initial matter, Applicants reaffirm election to prosecute claims 1-20. Claims 1-2 and 7-11 have been amended. New claim 47 has been added. No new matter has been added. Thus, claims 1-20 and 47 remain pending in the present application.

With regard to independent claim 1, Applicants describe and claim forming a gate dielectric above a surface of the substrate, forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region, and forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. With regard to independent claim 11, Applicants further describe and claim forming a source/drain extension adjacent the doped-poly gate structure and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

In the Office Action, claim 1 was rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Lee (U.S. Patent No. 5,360,751). The Examiner's rejections are respectfully traversed.

Lee is understood to describe a floating gate poly 52 that is lightly doped. In one embodiment, an angled implant heavily dopes one edge of the floating gate poly 56. See Lee, col. 5, ll. 2-14 and Figure 5. In a second embodiment, an angled implant heavily dopes both sides of the floating gate poly 56. However, Lee is completely silent with regard to, and teaches directly away from, Applicants' disclosed method of forming dopant-depleted regions. In fact, Lee teaches increasing the dopant concentration of the edges of the floating gate poly 56. For example, Lee states that the floating gate poly 52 is lightly doped to a concentration of 10^{16} - 10^{18}

atoms/cm³ and the angled implant heavily dopes the edge regions of the floating gate poly 56 to a concentration of 10¹⁹-10²¹ atoms/cm³. Furthermore, Lee is completely silent with regard to forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. As thus understood, Applicants respectfully submit that the present invention is not anticipated by Lee and request that the Examiner's rejection of claim 1 be withdrawn.

In the Office Action, claims 1-7 and 11-17 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Thompson, et al (U.S. Patent No. 6,020,244). The Examiner's rejections are respectfully traversed.

Thompson is understood to describe a gate 20 that is formed so that it is insulated from a substrate 30 by an insulative layer 27. Spacers 21 and 22 are then formed along opposite sides of the gate 20 and used to define shallower extensions of the source and drain regions 23, 24. See Thompson, col. 2, ll. 31-42 and Figure 2. A p-type region 25, which is more heavily doped than the substrate 30, is formed between the source and drain regions 23, 24. See Thompson, col. 2, ll. 45-48 and Figure 2. The region 25 is formed by ion implantation at a very high tilt angle using alight dopant species implanted at a relatively high energy. In particular, Thompson teaches implanting ions having an energy level of 10-20 KeV. This is done to force the dopant beneath the gate and into the central region of the channel. See Thompson, col. 3, ll. 11-38 and Figure 3.

The Examiner admits, in item 4 of the Office Action, that Thompson does not disclose forming a dopant-depleted region in the edge region of the doped-poly gate structure. However, the Examiner alleges that the Applicants' claimed dopant-depleted region would inherently be

formed because the dopant taught by Thompson passes through the edge regions. Applicants respectfully disagree. As is known to those of ordinary skill in the art, dopants may be implanted at varying locations and/or depths by varying the implant energy of the dopant. Thompson explicitly teaches implanting the dopant at a relatively high energy, such as an energy level of 10-20 KeV, to force the dopant beneath the gate and into the central region of the channel. See Thompson, col. 3, ll. 11-38 and Figure 3. Thus, the Applicants' claimed dopant-depleted region, *i.e.* in the edge region of the doped-poly gate structure adjacent the gate dielectric or in the substrate under the edge region of the doped-poly gate structure, would not inherently be formed by the process described in Thompson. In contrast, Applicants describe forming the first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and the second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. For example, Applicants describe, and claim in dependent claims 8 and 18, implanting the dopant at an implant energy ranging from about 0.2-5 keV. Thus, Applicants respectfully submit that the present invention is not anticipated by Thompson and request that the Examiner's rejection of claims 1-7 and 11-17 be withdrawn.

In the Office Action, claims 1-2 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Son, et al. (U.S. Patent No. 6,103,562). The Examiner's rejections are respectfully traversed.

Son is understood to describe a first gate electrode 25e between isolating regions 33. First conductive counter-doping regions 25c are formed at edge regions of the first gate electrode 25e. However, Son is completely silent with regard to the second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. Thus, Applicants respectfully

submit that the present invention is not anticipated by Son and request that the Examiner's rejection of claims 1 and 2 be withdrawn.

In the Office Action, claims 2, 8, and 10 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lee in view of Son. Claims 8-10 and 18-20 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Thompson in view of Son. The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the

claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002) (copy attached). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

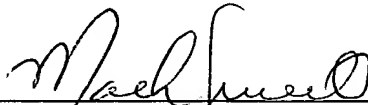
For at least the aforementioned reasons, it is respectfully submitted that the cited prior art references, either alone or in combination, fail to teach or suggest all the limitations of the present invention. Furthermore, there is no suggestion or motivation to modify the cited prior art to arrive at the Applicants' claimed invention, or any expectation of success to be found in the cited prior art. For example, Lee teaches away from forming a dopant-depleted region in the gate structure by teaching forming a heavily doped region in the edges of the floating gate poly 56, *i.e.* Lee teaches increasing the dopant concentration of the edges of the floating gate poly 56. For another example, Thompson teaches implanting the dopant at a relatively high energy to force the dopant beneath the gate and into the central region of the channel. There is no suggestion or motivation in the cited prior art to modify the implant energy taught by Thompson to form dopant-depleted regions in the edge region of the doped-poly gate structure and/or in the substrate under the edge region of the doped-poly gate structure, as claimed in the present invention. The Examiner relies on Son to teach specific dopant concentrations. Son, however, does not remedy the aforementioned deficiencies. Thus, Applicants respectfully submit that the present invention is not obvious in view of the cited prior art and request that the Examiner's rejections under 35 U.S.C. § 103(a) be withdrawn.

New claim 47 has been added to further define Applicants' invention. It is believed that claim 47 is also allowable over the prior art of record.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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AGENT FOR APPLICANTS

AMENDED AND NEW CLAIMS FOR SERIAL NO. 09/784,629

1. (Amended) A method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted[-poly] region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure.

2. (Amended) The method of claim 1, wherein forming the first dopant-depleted[-poly] region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the second dopant-depleted region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure.

7. (Amended) The method of claim 1, wherein forming the first and second dopant-depleted[-poly] regions includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure and depleting the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers.

8. (Amended) The method of claim 2, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure and the substrate under the edge region includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure and the substrate under the edge region, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm² to about 1.0×10^{15} ions/cm² at an implant energy ranging from about 0.2-5 keV.

9. (Amended) The method of claim 3, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure and the substrate under the edge region includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure and the substrate under the edge region, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm² to about 1.0×10^{15} ions/cm² at an implant energy ranging from about 0.2-5 keV.

10. (Amended) The method of claim 1, wherein forming the first dopant-depleted[-poly] region in the edge region of the doped-poly gate structure includes forming the first dopant-depleted[-poly] region to have a depth from the edge of the doped-poly gate structure, the depth of the first dopant-depleted[-poly] region ranging from about 50 Å-100 Å.

11. (Amended) A method comprising:

forming a gate dielectric above a surface of [the] a substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;
forming a source/drain extension (SDE) adjacent the doped-poly gate structure;
and
forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

47. (New) A method, comprising:

forming a gate dielectric above a surface of a semiconductor substrate;
forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and
forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure by:
implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric; and
forming depleting dielectric spacers adjacent the doped-poly gate structure.